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Encoding scheme minimizes errors in photonic converters

Mylene Arvizo, James Calusdian, Ken Hollinger, and Phillip E. Pace

A new scheme with an inherent integer Gray code property reduces photonic analog-to-digital converter errors while enhancing resolution.

Digitizing wideband radio frequency (RF) signals directly at the antenna is important in defense systems such as electronic warfare digital receivers and electronic signal intelligence collectors. It can eliminate the need for down-conversion to intermediate frequencies that cause spurious signals at the output of the receiver's analog-to-digital converter (ADC). Digitization also can hide any low power signals of interest. Integrated optical ADCs that use a parallel arrangement of wideband (bandwidth >50GHz) Mach-Zehnder modulators (MZMs) provide a solution by efficiently coupling the high-frequency RF energy into the optical domain without requiring down-conversion.[1] Using mode-locked lasers for sampling (pulse repetition frequency >300Gb/s) and having wideband photodetectors at the MZM output allows direct digitization of the high-frequency signals.[2]

Traditionally, each MZM in the parallel arrangement folds the RF input signal symmetrically, with each subsequent folding period doubled.[3] The electrical output from each detector is then quantized with a single comparator. When the detector output voltage crosses the comparator's matching

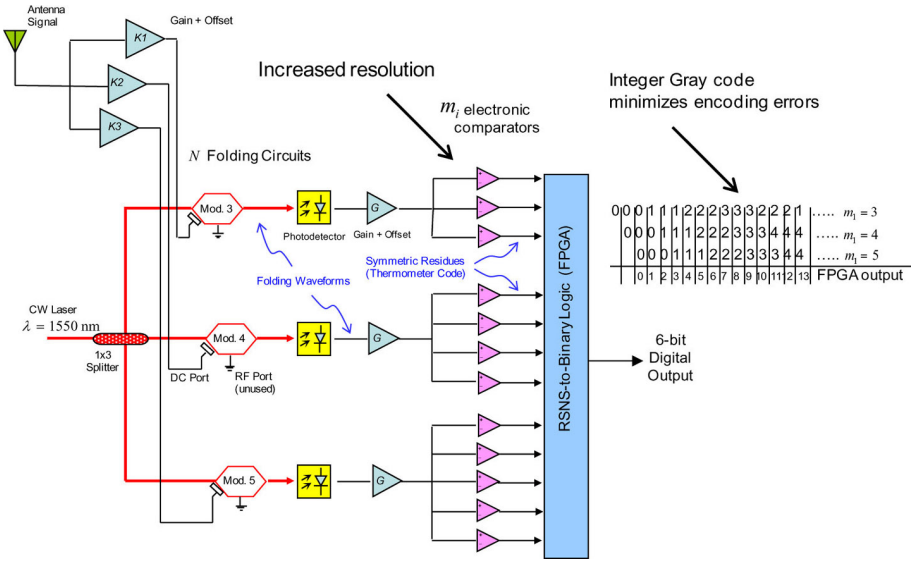

Figure 1. *Robust symmetrical number system photonic analog-to-digital converter with greater than 1 bit per interferometer. FPGA: Field programmable gate array. K1, K2, K3: Amplifiers to supply gain and offset voltages. CW laser: Continuous wave laser. G: Post-detection amplifier gain. Mod., m_i: Modulus. RSNS: Robust symmetrical number system.*

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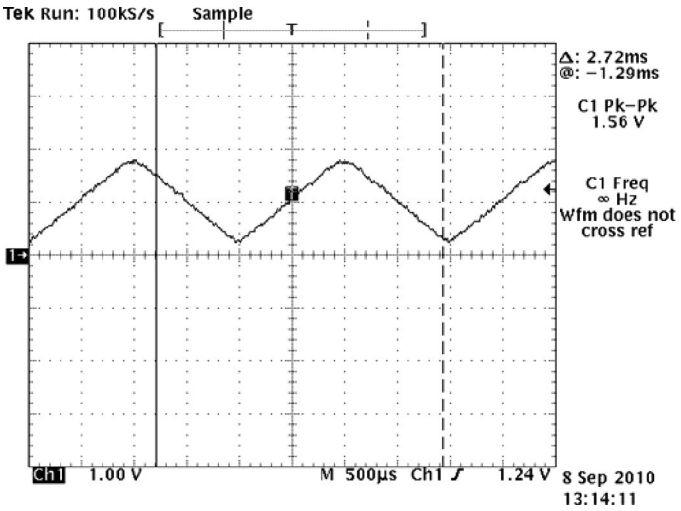

Figure 2. *Digital-to-analog converter output using the prototype device with a triangular input. This is an oscilloscope trace. C1: Trace one on the scope. Pk-Pk: Peak-to-peak. Ch1: Channel one. Wfm: Waveform.*

threshold voltage, the comparator output changes from a logic 0 to a logic 1. Together, the comparators represent the RF voltage in a binary format with one-bit per MZM/detector combination. Unfortunately, the achievable resolution is limited to 3 or 4 bits because of the MZM device capacitance.

We have developed a new modular preprocessing technique based on the robust symmetrical number system (RSNS) that can both increase the devices' resolution and minimize encoding errors.[4,5] The RSNS is composed of $N \geq 2$ moduli m_i that are co-prime (that is, the greatest common divisor is one). The RSNS preprocessing folds the signal in accordance with the modulus m_i. Instead of one comparator at each MZM detector's output, we used a parallel array of m_i comparators to analyze the detector's output amplitude.

Figure 1 shows the RSNS photonic ADC for $N = 3$ with $m_i \in \{3, 4, 5\}$, as well as integer values within each modulus (or comparator states), including a left shift. An example of the decimal output h from a field programmable gate array is also shown.[6] For this example, the length of paired terms without ambiguities (dynamic range) is $\hat{M} = 43$, and the position begins at the decimal value of $h = 61$ (not shown). The paired terms in each vector change one at a time at the next code position, resulting in an integer Gray (reflected binary) code property. That is, only one comparator changes state between any two code transitions.

The input signal's novel folding and the m_i comparators at the detector output extend the photonic MZM resolution beyond 1 bit per interferometer. The inherent Gray code property also makes it particularly attractive for error control. With the RSNS preprocessing, encoding errors resulting from comparator thresholds not being crossed simultaneously are eliminated, and interpolation circuitry can be removed.

We built a prototype device following this design. The input was a triangular waveform and the output was provided as input to a digital-to-analog converter (see Figure 2). To increase the resolution of a photonic ADC—while minimizing the encoding errors—we introduced a new technique based on a robust symmetrical number system encoding. We designed and constructed a prototype ADC to evaluate the concept's feasibility. Instead of one comparator at each detector's output, we used several comparators. The comparator states, when considered together, change one at a time at the next code position (integer Gray code property) and make the concept particularly attractive for error control. As a result, the RSNS has the important property that the largest nonlinearity is always less than a least significant bit. Our next step is to build a wideband, high-resolution device capable of achieving 12 bits of resolution over a 10GHz bandwidth.

Author Information

Mylene Arvizo
Naval Surface Warfare Center (NSWC)
Port Hueneme, CA

Mylene Arvizo holds an MS in electrical engineering and is currently a Littoral Combat Ship project officer at NSWC. She has served with the US Navy in Guam, and had sea duty tours including Yokusuka, Japan. Before the Naval Postgraduate School, she served as a requirements analyst on the staff of the Commander, Naval Surface Forces.

James Calusdian
Department of Electrical and Computer Engineering
Naval Postgraduate School
Monterey, CA

James Calusdian holds a PhD and MS in electrical engineering from the Naval Postgraduate School. Currently, he is part of the technical staff at that school's Control Systems Laboratory and the Optical Electronics Laboratory. He previously worked as an instrumentation engineer and a flight test engineer at the Air Force Flight Test Center at Edwards Air Force Base, CA.

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Ken Hollinger
Marine Tactical Systems Support
Camp Pendleton, CA

Kenneth Hollinger received an MS in electrical engineering from the Naval Postgraduate School, Monterey in 2009. Since August 1990 he has served in the Marine Corps in a variety of billets including M1A1 Tank Crewman, Motor Transport Operator, Supply Admin Clerk, Electronic Countermeasures Officer, Deputy Assessments Officer, and Command and Control Systems Chief Engineer. He is a member of Eta Kappa Nu, and his major interests are computer architecture, reconfigurable computing, artificial intelligence, and quantum computing.

Phillip E. Pace
Naval Postgraduate School
Monterey, CA

Phillip Pace is a professor, Department of Electrical and Computer Engineering.

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